Claims

What is claimed is:

1. A Complementary Metal Oxide Semiconductor (CMOS) bi-directional current mode differential link comprising:

a CMOS driver receiving a data input and having an output coupled to a transmission line;

a CMOS replica driver receiving said data input and providing a replica driver output substantially equal to said CMOS driver output;

a CMOS receiver coupled to both said transmission line and replica driver output; said CMOS receiver comprising a resistor summing network and a differential amplifier; and

said CMOS driver and said CMOS replica driver including a plurality of parallel current sources; each of said current sources being arranged to send positive or negative current through a load responsive to an applied control signal.

2. The CMOS bi-directional current mode differential link of Claim 1, wherein said resistor summing network comprises:

a first resistor, a first end of said first resistor being coupled to a positive phase output node of said CMOS driver;

a second resistor, a first end of said second resistor being coupled to a second end of said first resistor, and a second end of said second resistor being coupled to a negative phase output of said replica driver;

a third resistor, a first end of said third resistor being coupled to a negative phase output of said CMOS driver; and

a fourth resistor, a first end of said fourth resistor being coupled to a second end of said third resistor, and a second end of said fourth resistor being coupled to a positive phase output of said replica driver .

3. The CMOS bi-directional current mode differential link of Claim 2, wherein said differential amplifier comprises:

a first input coupled to a first node comprising said second end of said first resistor and said first end of said second resistor; and

a second input coupled to a second node comprising said second end of said third resistor and said first end of said fourth resistor.

4. The CMOS bi-directional current mode differential link of Claim 2, wherein said first resistor, said second resistor, said third resistor, and said fourth resistor are each of resistance magnitude at least ten times the characteristic impedance of said transmission line.

5. The CMOS bi-directional current mode differential link of Claim 2, further comprising:

a first capacitor, a first end of said first capacitor being coupled to said first input of said differential amplifier, and a second end of said first capacitor being coupled to ground; and

a second capacitor; a first end of said second capacitor being coupled to said second input of said differential amplifier, and a second end of said second capacitor being coupled to ground.

6. The CMOS bi-directional current mode differential link of Claim 2, wherein at least one of said first, second, third, and fourth resistors is split into a plurality of series-connected resistors, each coupling of two of said series-connected resistors defining an inter-resistor node.

7. The CMOS bi-directional current mode differential link of Claim 6, wherein at least one instant node of said inter-resistor nodes is further coupled to a first end of an inter-resistor capacitor instance unique to the instant node, and where a second end of each said inter-resistor capacitor instance is coupled to ground.

8. A method of receiving signals in a CMOS bi-directional current mode differential link, wherein said link comprises a data driver receiving a data input and having an output coupled to a first end of a transmission line; a replica driver receiving said data input and providing a replica driver output substantially equal to said data driver output; a receiver comprising a resistor-summing network and a differential amplifier; and said data driver and said replica driver including a plurality of parallel current sources; each of said current sources in said plurality of current sources being arranged to send positive or negative current through a load responsive to an applied control signal; said receiver capable of receiving a signal sent from a similar link coupled to a second end of said transmission line; said method comprising the steps of:

coupling a positive phase output of said data driver to a first end of a first resistor in said resistor-summing network;

coupling a second end of said first resistor to a first input of said differential amplifier, and further coupling said second end of said first resistor to a first end of a second resistor in said resistor-summing network;

coupling a second end of said second resistor to a negative phase output of said replica driver;

coupling a negative phase output of said data driver to a first end of a third resistor in said resistor-summing network;

coupling a second end of said third resistor to a second input of said differential amplifier, and further coupling said second end of said third resistor to a first end of a fourth resistor in said resistor-summing network; and

coupling a second end of said fourth resistor to a positive phase output of said replica driver.

9. The method of Claim 8, further comprising the step of splitting at least one of said first, second, third, and fourth resistors into two or more series-coupled resistors; each coupling of series-coupled resistors constituting an instance of an inter-resistor node.

10. The method of Claim 8, further comprising the step of coupling a first end of a first capacitor to said first input of said differential amplifier; and coupling a second end of said first capacitor to ground.

11. The method of Claim 8, further comprising the step of coupling a first end of a second capacitor to said second input of said differential amplifier; and coupling a second end of said second capacitor to ground.

12. The method of Claim 9, further comprising the step of coupling a first end of an instance capacitor to at least one instant node of said inter-resistor nodes, said instance capacitor being unique to each said inter-resistor node; and coupling a second end of each said instance capacitor to ground.